App. Serial No. 10/596,455 Docket No.: FR030154US1

## In the Claims:

Please amend claims 1-2 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A circuit comprising:

a plurality of interconnected logic blocks (100, 200, 300);

a main clock generator for distributing a reference clock signal (clk\_ref) to the logic blocks;

at least one local clock generator (110, 210, 310) in each logic block for generating a respective set of synchronized local clock signals (elk1\_phi1, elk2\_phi2) from the reference clock signal for further provision to respective elements (120, 130) of the logic block;

wherein a set of local clock signals of a first block is phase shifted relative to a set of local clock signals of a second block.

- 2. (Currently amended) The circuit of claim 1, wherein the first and second blocks communicate via a one-way data path (400).
- 3. (Original) The circuit of claim 2, wherein the first block comprises a first logic cell configured to write data onto the one-way data path on a rising edge of one of the local clock signals of the first block provided at an enable input of the first logic cell and the second block comprises a second logic cell configured to read the written data from the one-way data path on a rising edge of one of the local clock signals of the second block provided at an enable input of the second logic cell.
- 4. (Original) The circuit of claim 2, wherein the first block comprises a first logic cell configured to write data onto the one-way data path on a rising edge of one of the local clock signals of the first block provided at an enable input of the first logic cell and the second block comprises a second logic cell configured to read the written data from the one-way data path on a falling edge of the reference clock signal provided at an enable input of the second logic cell.

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5. (Original) The circuit of claim 1, further comprising at least two additional blocks that communication via a two-way data bus and wherein respective sets of local clock signals of the at least two additional logic blocks are synchronized with each other.